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EXAMINER	
MCCOMMAS, STUART S	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,950	NUMAO, TAKAJI	
	Examiner	Art Unit	
	Stuart McCommas	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/15/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 15-23 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson et al. (United States Patent 6,229,506), hereinafter referenced as Dawson, in view of Kimura (United States Patent Application 2004/0080474), hereinafter referenced as Kimura, and further in view of Yumoto (United States Patent 6,859,193), hereinafter referenced as Yumoto.

Regarding claim 15, Dawson discloses a display apparatus including a current driving light emitting element (OLED 380) and a driving transistor (365), the display apparatus comprising:

a first switching transistor (370) for connecting (i) a current control terminal of the driving transistor to (ii) a current output terminal of the driving transistor (column 4 lines 41-64; figure 3);

a first capacitor (Cs), connected to the current control terminal of the driving transistor (figure 3);

a second capacitor (Cc), having a first terminal connected to the current control terminal of the driving transistor (figure 3).

However Dawson fails to disclose a second switching transistor for connecting a second terminal of the second capacitor to the current output terminal of the driving transistor via a wire or a transistor, the second terminal being a terminal opposite to the first terminal, and a third switching transistor for connecting the second terminal of the second capacitor to a voltage line, wherein the second terminal of the second capacitor is connected to a node between the second and third switching transistors, the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element.

In a similar field of endeavor Kimura discloses a second switching transistor (1817) for connecting a second terminal of the second capacitor (1811) to the current output terminal of the driving transistor (1809) via a wire or a transistor, where the second terminal is opposite to the first terminal of the capacitor, and a third switching transistor (1807) for connecting the second terminal of the second capacitor to a voltage line, wherein the second terminal of the second capacitor is connected to a node between the second and third switching transistors, the voltage line being set to a value which corresponds to an anode potential of the current driving light emitting element when the image is displayed (paragraphs 145-155; figures 18-19).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dawson with Kimura by specifically providing a second switching transistor for connecting a second terminal of the second capacitor to the current output terminal of the driving transistor via a wire or a transistor, the second terminal being a terminal opposite to the first terminal, and a third switching transistor

for connecting the second terminal of the second capacitor to a voltage line, wherein the second terminal of the second capacitor is connected to a node between the second and third switching transistors the voltage line being set to a value which corresponds to an anode potential of the current driving light emitting element for the purpose of countering degradation in the EL element and for precisely controlling current output of a transistor to improve the quality of the display (paragraph 145).

In a similar field of endeavor Yumoto discloses the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element (column 14 lines 37-67; column 15 lines 1-63; figures 9-10).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dawson with Yumoto by specifically providing the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element for the purpose of precisely controlling the anode and cathode voltage of the display element (column 15 lines 4-63).

Regarding claim 16, Dawson, Kimura and Yumoto, the combination discloses everything as applied above, further Dawson discloses that during a first period within a current writing period of the driving transistor (365) the first switching transistor (370) connects the current control terminal to the current output terminal and during a second period within the current writing period the first switching transistor (360) disconnects the current control terminal from the current output terminal and during a readout period of the driving transistor the driving transistor supplies a current to the current light

emitting element (column 4 lines 41-67; column 5 lines 1-31; figure 3), and Kimura discloses that during a first period within a current writing period of the driving transistor the second switching transistor (1817) disconnects the second terminal and the current output terminal from each other (figures 18-19), and that the third switching transistor (1807) connects the second terminal to the voltage line (figures 18-19). Further Kimura discloses that during a second period within the current writing period the third switching transistor (1807) disconnects the second terminal from the voltage line (figure 19) and the second switching transistor (1817) connects the second terminal to the current output terminal, and that during a readout period of the driving transistor the second switching transistor disconnects the second terminal from the current output terminal, , the second switching transistor operating in an opposite logic state from the third switching transistor in the first and second periods (paragraphs 145-155; figures 18-19).

Regarding claim 17, Dawson and Kimura and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cs), the second capacitor (Cc) and the first switching transistor (370) are provided in each pixel circuit (figure 3), and Kimura discloses that the second switching transistor and the third switching transistor are provided in each pixel circuit (figures 18-19).

Regarding claim 18, Dawson and Kimura and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cs), the second capacitor (Cc) and the first switching transistor (370) are provided in each pixel circuit (figure 3), and Kimura discloses that the second switching transistor and the third switching transistor are provided outside the pixel circuit which portion

includes a source driver circuit (figures 18-19).

Regarding claim 19, Dawson and Kimura and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the light emitting element (380), the first capacitor (Cs), and the driving transistor (365) are provided in each pixel circuit and a connecting wire for connecting the current control terminal of the driving transistor (365) to the first terminal of the second capacitor (figure 3), and Kimura discloses that the second capacitor, the second switching transistor and the third switching transistor are provided outside the pixel circuit which portion includes a source driver circuit (figures 18-19).

Regarding claim 20, Dawson and Kimura and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the light emitting element (380), the first capacitor (Cs), and the driving transistor (365) are provided in the pixel circuit and that the first switching transistor (370) is provided outside the pixel circuit (figure 3), and Kimura discloses that the second capacitor is provided outside the pixel circuit and that the second switching transistor and the third switching transistor are provided as a part of the source driver circuit (figures 18-19), and a connecting wire for connecting the second terminal of the second capacitor to the second switching transistor and the third switching transistor (figures 18-19).

Regarding claim 21, Dawson and Kimura and Yumoto the combination discloses everything as applied above, further Dawson discloses that the light emitting element (380), the first capacitor (Cs), the second capacitor (Cc), the driving transistor (365), and the first switching transistor (370) are provided in each pixel circuit (figure 3), and

Kimura discloses that the second switching transistor and the third switching transistor are provided outside the pixel circuit, and a connecting wire for connecting the second terminal of the second capacitor to the current output terminal of the driving transistor (figures 18-19).

Regarding claim 22, Dawson and Kimura and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cs), the second capacitor (Cc) and the first switching transistor (370) are provided in each pixel circuit (figure 3), and Kimura discloses that the second switching transistor and the third switching transistor are provided in each pixel circuit (figures 18-19).

Regarding claim 23, Dawson and Kimura and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cs), the second capacitor (Cc) and the first switching transistor (370) are provided as a source driving circuit (figure 3), and that each of the pixel circuits includes a transistor (375) for controlling a current that is to be supplied to the current driving light emitting element (figure 3), and Kimura discloses that the second switching transistor and the third switching transistor are provided in a source driving circuit (figures 18-19).

Regarding claim 33, Dawson discloses a method for driving a display apparatus including a current driving light emitting element (380) and a driving transistor (365), the method comprising the steps of:

electrically connecting a current control terminal of the driving transistor to a first terminal of a first capacitor (figure 3);

electrically connecting, during a current writing period of the driving transistor, the

first terminal of the first capacitor to a first terminal of a second capacitor (column 4 lines 41-67; column 5 lines 1-31; figure 3);

during a first period, electrically connecting the current control terminal of the driving transistor to a current output terminal of the driving transistor, and causing the first capacitor and the second capacitor to retain a current control terminal potential that the driving transistor has on this occasion, where the second terminal is a terminal opposite to the first terminal (column 4 lines 41-67; column 5 lines 1-31; figure 3);

during a second period, correcting the current control terminal potential by disconnecting the current control terminal of the driving transistor from the current output terminal of the driving transistor by a first switching transistor (P3) and causing the first capacitor to retain the current control terminal potential that the driving transistor has on this occasion (column 4 lines 41-67; column 5 lines 1-31; figure 3);

controlling, during a current readout period of the driving transistor, an output current of the driving transistor with the use of the current control terminal potential, retained by the first capacitor, of the driving transistor (column 4 lines 41-67; column 5 lines 1-31; figure 3).

However Dawson fails to disclose during a first period, electrically connecting a second terminal of the second capacitor to a voltage line by a third switching transistor, electrically connecting the current control terminal of the driving transistor to a current output terminal of the driving transistor by a second switching transistor, and wherein the second terminal of the second capacitor is connected to a node between the second and third switching transistors, and correcting the control terminal potential by changing

electric connection of the second terminal of the second capacitor from the voltage line to the current output terminal of the driving transistor by the second and third transistors, the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element.

In a similar field of endeavor Kimura discloses during a first period, electrically connecting a second terminal of the second capacitor (1811) to a voltage line by a third switching transistor (1807), electrically connecting the current control terminal of the driving transistor to a current output terminal of the driving transistor by a second switching transistor (1818), and wherein the second terminal of the second capacitor is connected to a node between the second and third switching transistors (figures 18-19), and correcting the control terminal potential by changing electric connection of the second terminal of the second capacitor from the voltage line to the current output terminal of the driving transistor by the second and third transistors (paragraphs 145-155; figures 18-19). Further Kimura discloses that the voltage line being set to a value which corresponds to an anode potential of the current driving light emitting element (figures 18-19).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dawson with Kimura by specifically providing during a first period, electrically connecting a second terminal of the second capacitor to a voltage line by a third switching transistor, electrically connecting the current control terminal of the driving transistor to a current output terminal of the driving transistor by a second switching transistor, and wherein the second terminal of the second capacitor is

connected to a node between the second and third switching transistors, and correcting the control terminal potential by changing electric connection of the second terminal of the second capacitor from the voltage line to the current output terminal of the driving transistor by the second and third transistors, and the voltage line being set to a value which corresponds to an anode potential of the current driving light emitting element for the purpose of countering degradation in the EL element and for precisely controlling current output of a transistor to improve the quality of the display (paragraph 145).

In a similar field of endeavor Yumoto discloses the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element (column 14 lines 37-67; column 15 lines 1-63; figures 9-10).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dawson with Yumoto by specifically providing discloses the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element for the purpose of precisely controlling the anode and cathode voltage of the display element (column 15 lines 4-63).

Regarding claim 34, Dawson and Kimura and Yumoto, the combination discloses everything as applied above, further Kimura discloses that during the second period, the electric connecting of the second terminal of the second capacitor to the current output terminal of the driving transistor is carried out before disconnecting the voltage line from the second terminal of the second capacitor (paragraphs 145-155; figures 18-19).

3. Claims 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura in view of Dawson and further in view of Yumoto.

Regarding claim 24, Kimura discloses a display apparatus including a current driving light emitting element (1812) and a driving transistor (1810), the display apparatus comprising:

a first switching transistor (1808) for connecting a current control terminal of the driving transistor to a current input terminal of the driving transistor (figures 18-19);

a second capacitor (1811), having a first terminal connected to the current control terminal of the driving transistor (figure 18);

a second switching transistor (1817) for connecting a second terminal of the second capacitor to the current input terminal of the driving transistor via a wire and a transistor, the second terminal being a terminal opposite to the first terminal, and a third switching transistor (1807) for connecting the second terminal of the second capacitor to a voltage line, wherein the second terminal of the second capacitor is connected to a node between the second and third switching transistors, and the voltage line being set to a value which corresponds to an anode potential of the current driving light emitting element (paragraphs 145-155; figures 18-19).

However Kimura fails to disclose a first capacitor connected to the current control terminal of the driving transistor and the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element.

In a similar field of endeavor Dawson discloses a first capacitor (Cc) and a second capacitor (Cs) connected to the current control terminal of the driving transistor (figure 3).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kimura with Dawson by specifically providing a first capacitor connected to the current control terminal of the driving transistor for the purpose of temporarily storing the data voltage and for storing voltage to compensate for threshold voltage variation to improve the quality of the display (column 1 lines 60-64).

In a similar field of endeavor Yumoto discloses the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element (column 14 lines 37-67; column 15 lines 1-63; figures 9-10).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kimura with Yumoto by specifically providing the voltage line being set to a value which corresponds to an anode potential from a property of the current driving light emitting element for the purpose of precisely controlling the anode and cathode voltage of the display element (column 15 lines 4-63).

Regarding claim 25, Kimura and Dawson and Yumoto, the combination discloses everything as applied above, further Kimura discloses that during a first period within a current writing period of the driving transistor (1810), the first switching transistor (1808) connects the current control terminal to the current input terminal (figure 32), the second

switching transistor (1817) disconnects the second terminal and the current output terminal from each other, and that the third switching transistor (1807) connects the second terminal to the predetermined voltage line, the second switching transistor operating in an opposite logic state from the third switching transistor in the first and second periods (figures 18-19), and that during a second period within the current writing period the first switching transistor (1808) disconnects the current control terminal from the current input terminal and the third switching transistor (1807) disconnects the second terminal from the voltage line (figures 18-19) and the second switching transistor (1818) connects the second terminal to the current input terminal (figures 18-19) and during a readout period of the driving transistor the second switching transistor (1818) disconnects the second terminal from the current input terminal and the driving transistor supplies a current to the current light emitting element (paragraphs 145-155; figures 18-19).

Regarding claim 26, Kimura and Dawson and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cc) is provided in each pixel circuit (figure 3), and Kimura discloses that the second capacitor (1811), the first switching transistor (1808), the second switching transistor (1818) and the third switching transistor (1807) are provided in each pixel circuit (paragraphs 145-155; figures 18-19).

Regarding claim 27, Kimura and Dawson and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cc) is provided in each pixel circuit (figure 3), and Kimura discloses that the second

capacitor (1811) and the first switching transistor (1808) and the second switching transistor (1818) and the third switching transistor (1807) are provided outside the pixel circuit which portion includes a source driver circuit (paragraphs 145-155; figures 18-19).

Regarding claim 28, Kimura and Dawson, and Yumoto the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cc) is provided in each pixel circuit (figure 3), and Kimura discloses that the light emitting element (1812) and the driving transistor (1810) are provided in each pixel circuit, and a connecting wire for connecting the current control terminal of the driving transistor to the first terminal of the second capacitor (figure 18), and Kimura discloses that the second capacitor (1811), the second switching transistor (1818) and the third switching transistor (1807) are provided outside the pixel circuit which portion includes a source driver circuit (paragraphs 145-155; figures 18-19).

Regarding claim 29, Kimura and Dawson and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cc) is provided in each pixel circuit (figure 3), and Kimura discloses that the light emitting element (1812) and the driving transistor (1810) are provided in each pixel circuit (figure 18), and Kimura discloses that the second capacitor (1811) and the first switching transistor (1808) are provided outside the pixel circuit and that the second switching transistor (1818) and the third switching transistor (1807) are provided as a part of the source driver circuit (figures 18-19), and a connecting wire for connecting the second terminal of the second capacitor to the second switching transistor and the third

switching transistor (paragraphs 145-155; figures 18-19).

Regarding claim 30, Kimura and Dawson and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cc) is provided in each pixel circuit (figure 3), and Kimura discloses that the light emitting element (1812), the first switching transistor, the second capacitor (1811) and the driving transistor (1810) are provided in each pixel circuit (figure 18), and Kimura discloses that the second switching transistor (1818) and the third switching transistor (1807) are provided outside the pixel circuit, and a connecting wire for connecting the second terminal of the second capacitor to the current input terminal of the driving transistor (paragraphs 145-155; figures 18-19).

Regarding claim 31, Kimura and Dawson and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cc) is provided in each pixel circuit (figure 3), and Kimura discloses that the second capacitor, the first switching transistor, the second switching transistor and the third switching transistor are provided in each pixel circuit (paragraphs 145-155; figures 18-19).

Regarding claim 32, Kimura and Dawson and Yumoto, the combination discloses everything as applied above, further Dawson discloses that the first capacitor (Cs) is provided as a source driving circuit (figure 3), and that each of the pixel circuits includes a transistor (375) for controlling a current that is to be supplied to the current driving light emitting element (figure 3), and Kimura discloses that the second capacitor (1811), the first switching transistor (1808), the second switching transistor (1818) and the third

switching transistor (1807) are provided in a source driving circuit (paragraphs 145-155; figures 18-19).

Response to Arguments

4. Applicant's arguments with respect to claim 15-34 have been considered but are believed to be answered by and therefore moot in view of the new ground(s) of rejection.

On pages 12-15 of Applicant's remarks, Applicant argues that Kimura does not disclose the second and third transistors operating in opposite logic states in the first and second periods.

The Examiner respectfully disagrees, because Kimura discloses in figures 19D-19F that the second transistor 1817 and the third transistor 1807 operate in opposite logic states for at least a period of time during the first and second time periods.

On pages 15-17 of Applicant's remarks, Applicant argues that transistors 1817 and 1807 in Kimura do not operate in the same manner as the instant invention during the time periods.

The Examiner respectfully disagrees, because Kimura as previously stated discloses the second transistor 1817 and the third transistor 1807 operate in opposite logic states for at least a period of time during the first and second time periods. In the first period the transistors operate in the opposite logic state depicted in figures 19B-19E, and in the second period the transistors operate in the opposite logic state depicted in figures 19D-19F.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stuart McCommas whose telephone number is (571)270-3568. The examiner can normally be reached on Monday-Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alex Eisen can be reached on 571-272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stuart McCommas
Patent Examiner
Art Unit 2629

SSM

/Alexander Eisen/
Supervisory Patent Examiner, Art Unit 2629